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 ** CONTINUING DATA ~~N~~ ^{VS} *****

 ** FOREIGN APPLICATIONS ^{VS} *****
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35 USC 119 (a-d) conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	COUNTRY	DRAWING	CLAIMS	CLAIMS
Verified and Acknowledged Examiner's Signature <u>[Signature]</u> Initials <u>VS</u>	JAPAN	17	22	6

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TITLE

Logic circuit optimizing method, logic circuit optimizing device and logic circuit composing device

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